Claims

What is claimed is:

1. A process for controlling a multiple core expander comprising:

using a test port of said multiple core expander to send operational codes to said multiple core expander to put all but one core of said multiple core expander in bypass mode;

serially reading data from, and serially writing data to, at least one internal register of said one core through said test port.

2. A method of controlling the operation of a dual expander having first and second expander cores by reading and writing control bits through a single test port in said dual expander comprising:

placing one of said first and second expander cores in bypass mode;

transmitting a serial data stream of said control bits through said test port to a shift register to generate a control byte;

parallel shifting said control byte from said shift register to a control register in one of said first and second expander cores that is not in bypass mode;

providing dummy bits as needed in said serial data stream to correctly form said control byte.

3. A process for performing a register write operation in a first expander core of a dual expander comprising:

serially shifting operational code bits into a test port, said operational code bits including instructions to place a second expander core, in said dual expander, in bypass mode;

generating an operational byte from said operational code bits;

placing said second expander core in bypass mode in response to said operational byte;

shifting a dummy bit into said test port;

serially shifting control bits, address bits and write command bits into said test port;

generating a control byte from said control bits and an address byte from said address bits;

writing said control byte to a register in said first expander core at an address indicated by said address byte.

4. A process for performing a register write operation in a second expander core of a dual expander comprising:

serially shifting operational code bits into a test port of said dual expander, said operational code bits including instructions to place a first expander core, in said dual expander, in bypass mode;

generating an operational byte from said operational code bits;

placing said first expander core in bypass mode in response to said operational byte;

shifting control bits, address bits and write command bits into said test port;

shifting a dummy bit into said test port;

generating a control byte from said control bits and an address byte from said address bits;

writing said control byte to a register in said second expander core at an address indicated by said address byte.

5. A process for performing a register read operation from a first expander core of a dual expander comprising:

serially shifting operational code bits into a test port of said dual expander, said operational code bits including instructions to place a second expander, in said dual expander, in bypass mode;

generating an operational byte from said operational code bits;

placing said second expander core in bypass mode in response to said operational byte;

shifting a dummy bit into said test port of said dual expander;

serially shifting read address bits and a read command into said test port of said dual expander;

generating an address byte from said read address bits;

serially reading data from a register in said first expander core at an address indicated by said address byte through said test port of said dual expander.

6. A process for performing a register read operation from a second expander core of a dual expander comprising:

serially shifting operational code bits into a test port of said dual expander, said operational code bits including instructions to place a first expander, in said dual expander, in bypass mode;

generating an operational byte from said operational code bits;

placing said first expander core in bypass mode in response to said operational byte;

serially shifting read address bits and a read command into a test port of said dual expander;

shifting a dummy bit into said test port of said dual expander;

generating a read address byte from said read address bits;

serially reading data from a register in said second expander core at an address indicated by said address byte through said test port of said dual expander.